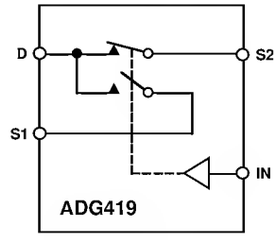
LC²MOS Precision Mini-DIP Analog Switch

ADG419

FEATURES
- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (< 35 Ω)
- Ultralow Power Dissipation (< 35 μW)
- Fast Transition Time (145 ns max)
- Break-Before-Make Switching Action
- Latch-Up Proof
- Plug-In Replacement for DG419

APPLICATIONS
- Precision Test Equipment
- Precision Instrumentation
- Battery Powered Systems
- Sample Hold Systems

FUNCTIONAL BLOCK DIAGRAM



SWITCH SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG419 is a monolithic CMOS SPDT switch. This switch is designed on an enhanced LC²MOS process which provides low power dissipation yet gives high switching speed, low on resistance and low leakage currents.

The on resistance profile of the ADG419 is very flat over the full analog input range ensuring excellent linearity and low distortion. The part also exhibits high switching speed and high signal bandwidth. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

Each switch of the ADG419 conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. The ADG419 exhibits break-before-make switching action.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG419 is fabricated on an enhanced LC²MOS, trench isolated process giving an increased signal range that extends to the supply rails.
2. Ultralow Power Dissipation
3. Low R_{ON}
4. Trench Isolation Guards Against Latch Up
   A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions
5. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG419 can be operated from a single rail power supply. The part is fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

REV. 0

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ADG419–SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	25		25		Ω typ	V_D = ±12.5 V, I_S = –10 mA
	35	45	35	45	Ω max	V_{DD} = +13.5 V, V_{SS} = –13.5 V
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±5	±0.25	±15	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.75	±5	±0.75	±30	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.4		±0.4		nA typ	V_S = V_D = ±15.5 V;
	±0.75	±5	±0.75	±30	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±0.005		±0.005	µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	145	200	145	200	ns max	R_L = 300 Ω, C_L = 35 pF; V_{S1} = ±10 V, V_{S2} = ∓10 V; Test Circuit 4
Break-Before-Make Time	30		30		ns typ	R_L = 300 Ω, C_L = 35 pF;
Delay, t_D	5		5		ns min	V_{S1} = V_{S2} = ±10 V; Test Circuit 5
OFF Isolation	80		80		dB typ	R_L = 50 Ω, f = 1 MHz; Test Circuit 6
Channel-to-Channel Crosstalk	70		70		dB typ	R_L = 50 Ω, f = 1 MHz; Test Circuit 7
C_S (OFF)	6		6		pF typ	f = 1 MHz
C_D, C_S (ON)	55		55		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
I_{DD}	0.0001		0.0001		µA typ	V_{IN} = 0 V or 5 V
	1	2.5	1	2.5	µA max	
I_{SS}	0.0001		0.0001		µA typ	
	1	2.5	1	2.5	µA max	
I_L	0.0001		0.0001		µA typ	V_L = +5.5 V
	1	2.5	1	2.5	µA max	

NOTES

[1]Temperature ranges are as follows: B Version: –40°C to +85°C; T Version: –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply (V_{DD} = +12 V ± 10%, V_{SS} = 0 V, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		0 to V_{DD}		0 to V_{DD}	V	
R_{ON}	40		40		Ω typ	V_D = +3 V, +8.5 V, I_S = –10 mA
		60		70	Ω max	V_{DD} = +10.8 V
LEAKAGE CURRENT						V_{DD} = +13.2 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = 12.2 V/1 V, V_S = 1 V/12.2 V;
	±0.25	±5	±0.25	±15	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = 12.2 V/1 V, V_S = 1 V/12.2 V;
	±0.75	±5	±0.75	±30	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.4		±0.4		nA typ	V_S = V_D = 12.2 V/1 V;
	±0.75	±5	±0.75	±30	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±0.005		±0.005	µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	170	250	170	250	ns max	R_L = 300 Ω, C_L = 35 pF; V_{S1} = 0 V/8 V, V_{S2} = 8 V/0 V; Test Circuit 4
Break-Before-Make Time Delay, t_D	60		60		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +8 V; Test Circuit 5
OFF Isolation	80		80		dB typ	R_L = 50 Ω, f = 1 MHz; Test Circuit 6
Channel-to-Channel Crosstalk	70		70		dB typ	R_L = 50 Ω, f = 1 MHz; Test Circuit 7
C_S (OFF)	13		13		pF typ	f = 1 MHz
C_D, C_S (ON)	65		65		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +13.2 V
I_{DD}	0.0001		0.0001		µA typ	V_{IN} = 0 V or 5 V
	1	2.5	1	2.5	µA max	
I_L	0.0001		0.0001		µA typ	V_L = +5.5 V
	1	2.5	1	2.5	µA max	

NOTES
[1]Temperature ranges are as follows: B Version: –40°C to +85°C; T Version: –55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

Table I. Truth Table

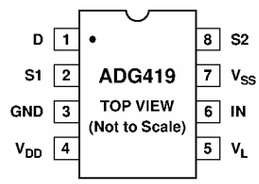
Logic	Switch 1	Switch 2
0	ON	OFF
1	OFF	ON

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG419BN	–40°C to +85°C	N-8
ADG419BR	–40°C to +85°C	SO-8
ADG419TQ	–55°C to +125°C	Q-8

*N = Plastic DIP, Q = Cerdip, SO = 0.15" Small Outline IC (SOIC).

PIN CONFIGURATION DIP/SOIC



ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} ..... +44 V
V_{DD} to GND ..... –0.3 V to +25 V
V_{SS} to GND ..... +0.3 V to –25 V
V_L to GND ..... –0.3 V to V_{DD} + 0.3 V
Analog, Digital Inputs[2] ..... V_{SS} – 2 V to V_{DD} + 2 V
or 30 mA, Whichever Occurs First
Continuous Current, S or D ..... 30 mA
Peak Current, S or D ..... 100 mA
(Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Extended (T Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
Cerdip Package, Power Dissipation ..... 600 mW
θ_{JA}, Thermal Impedance ..... 110°C/W
Lead Temperature, Soldering (10 sec) ..... +300°C
Plastic Package, Power Dissipation ..... 400 mW
θ_{JA}, Thermal Impedance ..... 100°C/W
Lead Temperature, Soldering (10 sec) ..... +260°C
SOIC Package, Power Dissipation ..... 400 mW
θ_{JA}, Thermal Impedance ..... 155°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.
V_L	Logic power supply (+5 V).
GND	Ground (0 V) reference.
S	Source terminal. May be an input or an output.
D	Drain terminal. May be an input or an output.
IN	Logic control input.
R_{ON}	Ohmic resistance between D and S.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	"OFF" switch source capacitance.
C_D, C_S (ON)	"ON" switch capacitance.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another.
t_D	"OFF" time or "ON" time measured between the 90% points of both switches when switching from one address state to the other.
V_{INL}	Maximum input voltage for logic "0."
V_{INH}	Minimum input voltage for logic "1."
I_{INL} (I_{INH})	Input current of the digital input.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" channel.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.

TRENCH ISOLATION

In the ADG419, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, the result being a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode which is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A silicon-controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch up. With trench isolation, this diode is removed, the result being a latch-up proof switch.

Trench isolation also leads to lower leakage currents. The ADG419 has a leakage current of 0.25 nA as compared with a leakage current of several nanoamperes in non-trench isolated switches.

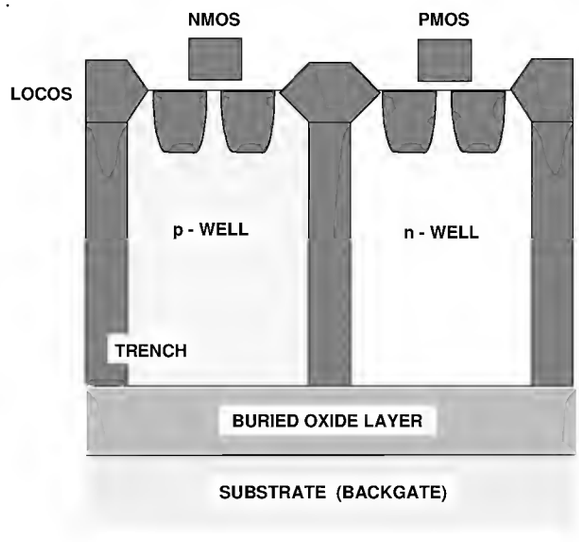


Figure 1. Trench Isolation

Typical Performance Graphs

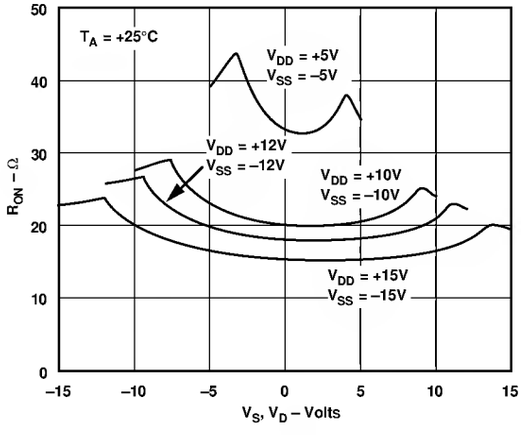


Figure 2. R_{ON} as a Function of V_D (V_S): Dual Supply Voltage

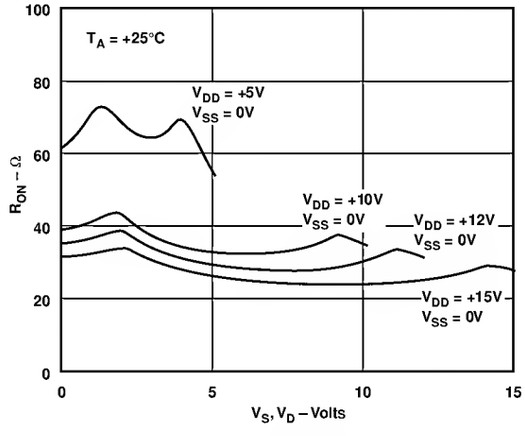


Figure 3. R_{ON} as a Function of V_D (V_S): Single Supply Voltage

Typical Performance Graphs

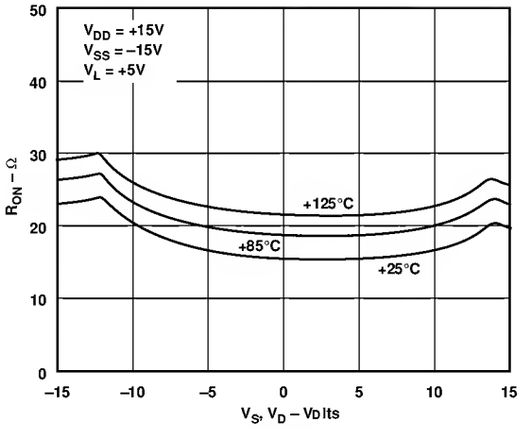


Figure 4. R_{ON} as a Function of V_D (V_S) for Different Temperatures

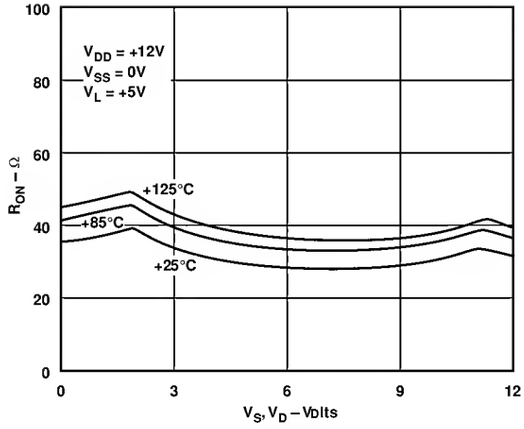


Figure 7. R_{ON} as a Function of V_D (V_S) for Different Temperatures

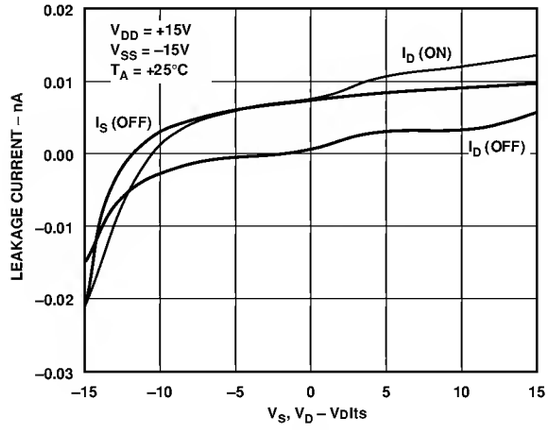


Figure 5. Leakage Currents as a Function of V_S (V_D)

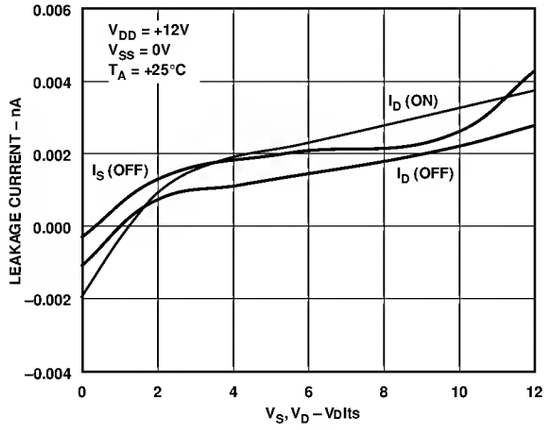


Figure 8. Leakage Currents as a Function of V_S (V_D)

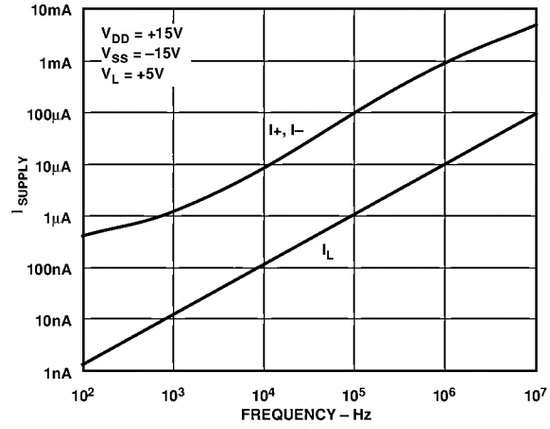


Figure 6. Supply Current vs. Input Switching Frequency

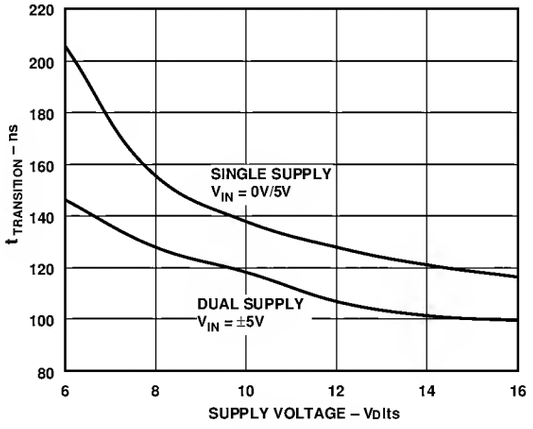
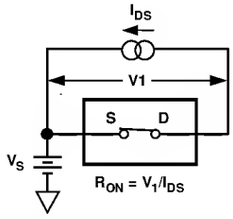
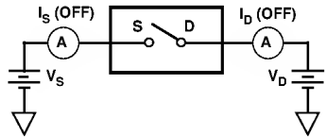


Figure 9. Transition Time vs. Power Supply Voltage

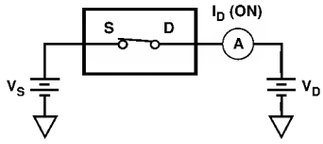
Test Circuits



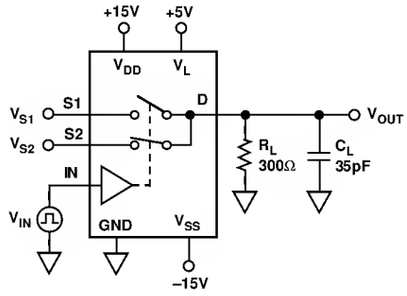
Test Circuit 1. On Resistance

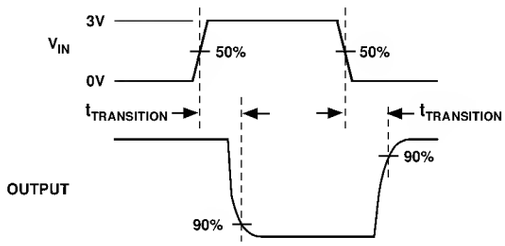


Test Circuit 2. Off Leakage

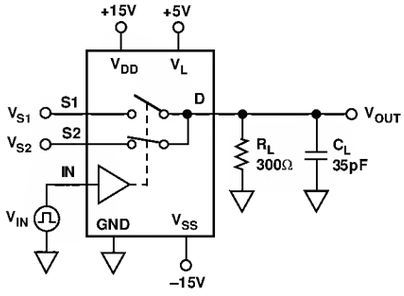


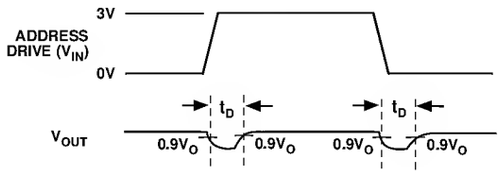
Test Circuit 3. On Leakage



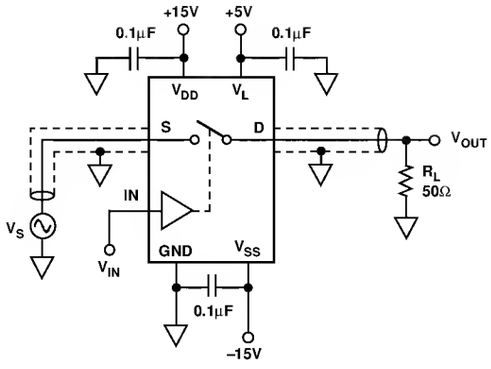


Test Circuit 4. Transition Time, $t_{TRANSITION}$

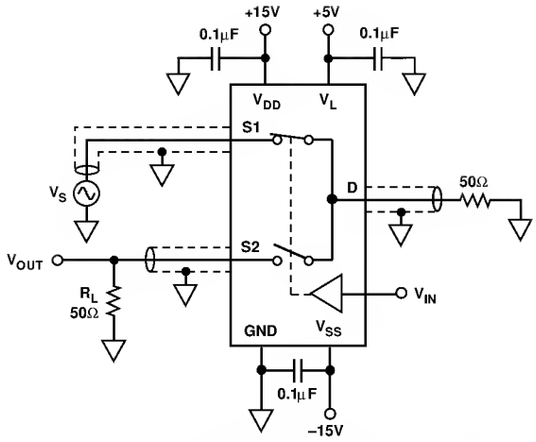




Test Circuit 5. Break-Before-Make Time Delay, t_D



Test Circuit 6. Off Isolation



CHANNEL TO CHANNEL CROSSTALK = 20 x LOG $|V_S/V_{OUT}|$

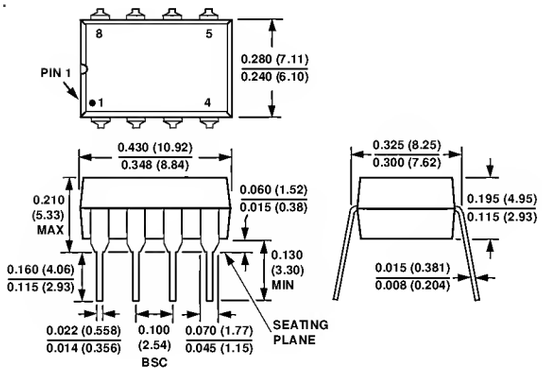
Test Circuit 7. Crosstalk

C1926–18–6/94

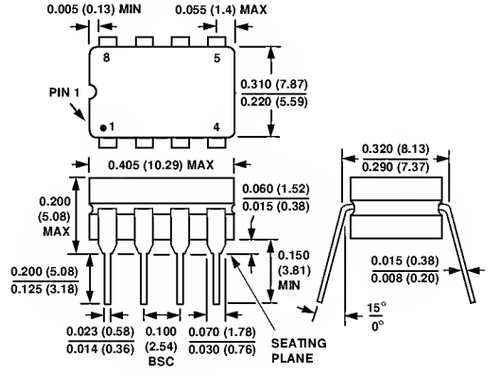
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

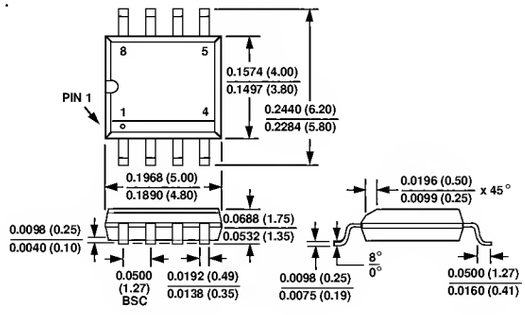
8-Pin Plastic DIP (N-8)



8-Pin Cerdip (Q-8)



8-Pin SOIC (SO-8)
(Narrow Body)



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